PlatformConference
Direction • Design • Perspective • Analysis

Advancing Southbridge Design with HyperTransport™ Interconnect Technology

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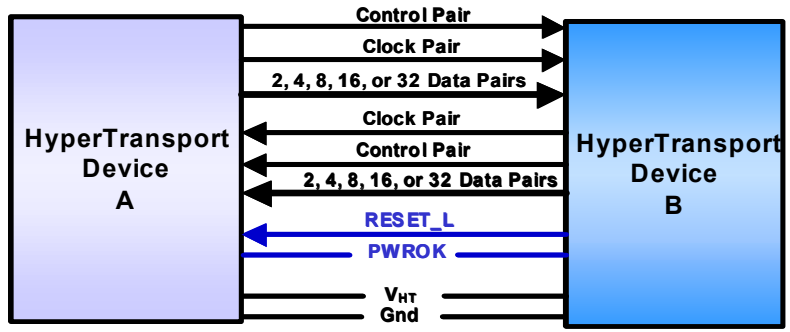
HyperTransport™

- Efficient chip-to-chip Interconnect
  - QoS & isochrony
    - Low latency with no data-encoding
    - Coherency option facilitates processor-to-processor communications
  - Scaleable bandwidth
    - By frequency (increment of 200MHz)
    - By bus-width of 2-, 4-, 8-, 16-, or 32-bit wide in each direction
  - Simpler I/Os
    - Differential
    - No clock recovery
  - Power-friendly
    - Each link can be configured to run at a multiple of 200MHz, up to max. 800MHz.

HyperTransport™ Basics

- A HT-bus has two uni-directional point-to-point Links
  - Each Link can be 2-, 4-, 8-, 16-, or 32-bit wide in each direction
- @ 800MHz clock, up to 3.2GB/s for 8-bit each-way Links
  - 24x the bandwidth of PCI-32/33 with less pins (55 vs. 84)
- Packets are multiple of 4-Bytes in length
- Serial link with commands, data and addresses use the same bits
- Signal to GND ratio ~ 4:1
- Optional Link power-down signals for mobile
  - HyperTransportDeviceStop_L, DevReq_L
  - Power per pin-pair is '0' when in HyperTransportDeviceStop mode
- PCI compatible



PWROK, RESET_L required for proper reset & initialization
V_{HT} routed between devices for proper common mode range

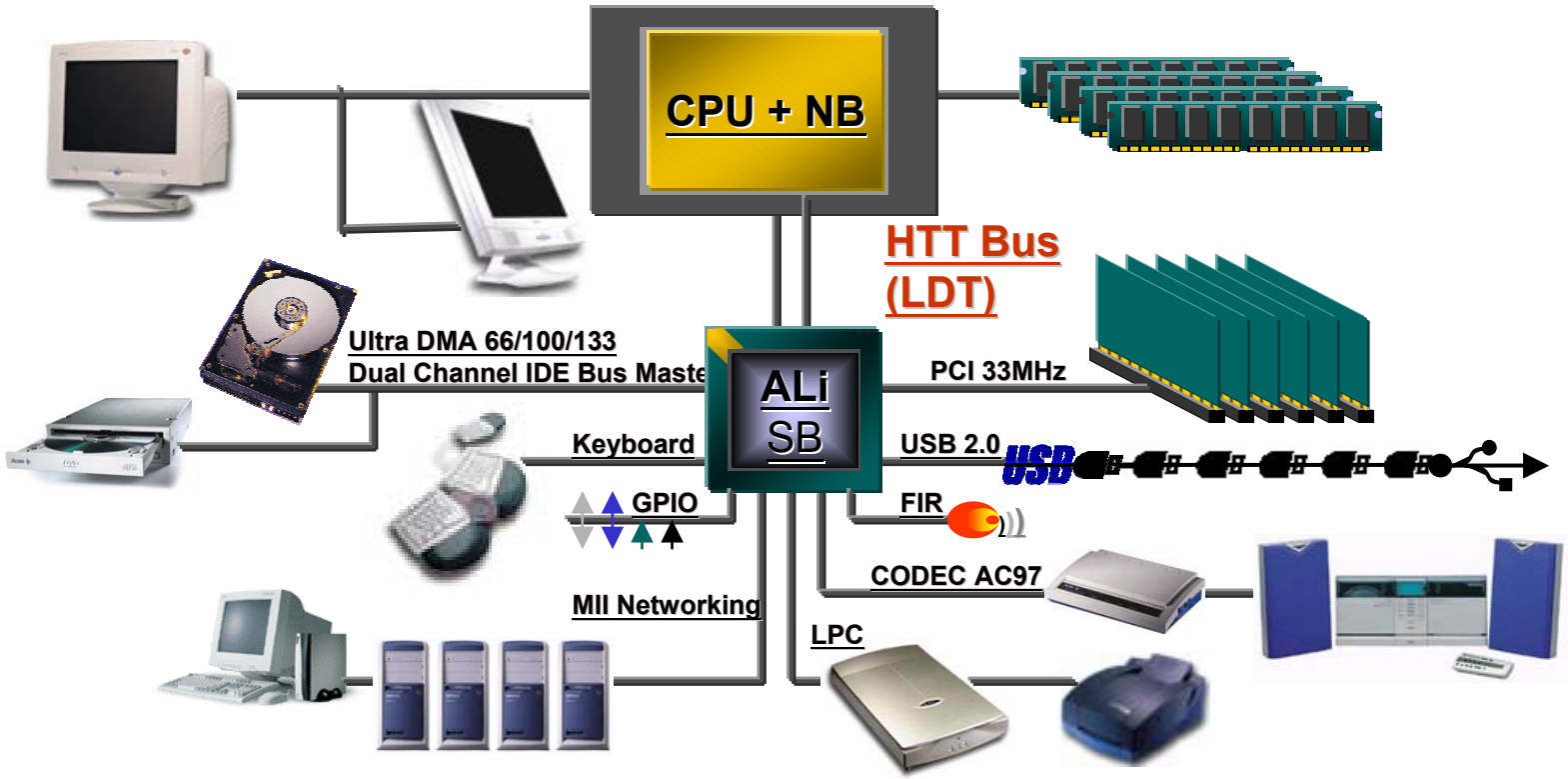
Bus Width (Each Way)	2	4	8	16	32
Data Pins (total)	8	16	32	64	128
Clock Pins (total)	4	4	4	8	16
Control Pins (total)	4	4	4	4	4
Subtotal (high speed)	**16**	**24**	**40**	**76**	**148**
VLDT	2	2	3	6	10
GND	4	6	10	19	37
PWROK	1	1	1	1	1
RESET_L	1	1	1	1	1
Total Pins	**24**	**34**	**55**	**103**	**197**
Total Max BW GB/s	**0.8**	**1.6**	**3.2**	**6.4**	**12.8**

DC Power per Pin-Pair: 4 ~ 9 mW, 6 $mW_{Typical}$
Signal to V_{HT}/Gnd Ratio: 4:1

HyperTransport™ Adoption

- CY2001
  - PC core logics chipsets since Q3CY01
  - Network processors from Broadcom & PMC-Sierra in Q4CY01
  - Key component of proposal for LA2 Look-at-Side I/F at Network Processor Forum
  - FPGA products from Altera
- Future
  - More PC core logics chipsets to be released
  - Applications across computing, embedded, CE segments
    - x86-, MIPS-based processors with integrated HT-bus
    - Network processors to be released: Sandcraft, ...
  - Magamacro from IP providers and design houses

ALi commitment to HTT



Note: ALi SB contains X86 style PMU

ALi HTT SB Key Spec

- HyperTransport™ Technology (HTT)
  - Lightning Data Transport (LDT)
    - 8-bit LDT links in each direction
    - At least 400 x 2 MB/s Data Transfer Rate
- PCI Spec. v2.2 Compliant
  - PCI 33MHz Slots (Supports up to 6 Req/Gnt Pairs)
- Enhanced DMA Controller, Interrupt Controller, Counters/Timers
- ACPI v2.0 Power Management Support
- Integrated IDE Controller Supports ATA 33/66/100/133
- USB Host Controllers with 6 Ports Support USB 1.1/2.0 Spec.

ALi HTT SB Key Spec Cont.

- AC97 v2.2 Controllers Support for Audio and Telephony Codecs.
  - Support up to 6 channels and SPDIF In/Out
- Integrated 10/100 Mb/s Fast Ethernet MAC
- Low Pin Count (LPC) Interface
- Integrated PS2/AT Keyboard controller and PS2 Mouse controller
- Integrated 256B SRAM Real Time Clock
- Integrated Fast Infra-Red Controller
- Integrated Memory Stick & Secure Digit Host Controller

Key Feature of Ethernet MAC

- Compliant with PCI spec. 2.2.
- Support PCI Bus power management interface Spec.1.1.
- Compliant with ACPI spec.2.0
- Support 1/10/100 Mbps transfer
- Support MII/RMII interface to PHY Transceiver chip
- Support Full/Half Duplex operation
- Support Home LAN interface
- Support Wake on LAN

Key Feature of IDE Controller

- PCI Spec. 2.2 & PCI Power Management Spec. 1.1 Compliant
- Supports Ultra DMA 33/66/100/133 Mode Transfers.
- Supports PIO Mode Up to Mode 5 Timings, and Multiword DMA Mode 0,1,2,3,4,5 with Independent Timing of Up to 4 Drives
- Deep Buffers for Each Channel
- Support Tri-state IDE Bus Signals for Swap Bay
- Independent Activity Monitoring for Each Drive

Key Feature of AC97 Audio Controller

- PCI Spec. 2.2
- PCI Power management Spec. 1.1 Compliant
- AC'97 CODEC 2.1 Compliant
- Independent Scatter Gather DMA Channels
  - 6 Playback Channels : PCM L/R, Surround L/R, Center and LFE
  - 1 Recording Channel
  - I2S Input/Output Channels
  - SPDIF Input/Output Channels
  - Microsoft WDM Streaming Architecture Compliant
- Support DirectSound, DirectSound3D, A3D and EAX APIs

Key Feature of AC97 Modem Controller

- PCI Spec. 2.2
- PCI Power Management Spec. 1.1 Compliant
- AC'97 2.1 Compliant Digital Controller Interface
- 4 Separate Telephony Bus master Channels.
- One for Modem Output, One for Modem Input,
- One for Handset Input, and One for Handset Output
- AC'97 2.1 GPIO Pins Status and Control Support
- Power Management and Wake-up Event Support (PME#)
- Caller ID String Transmission via AC-link Support

Key Feature of USB Controller

- PCI Spec. 2.2
- PCI Power Management Spec. 1.1 Compliant
- 3 OHCI 1.1 host controller with 6 USB Ports
- 1 EHCI USB 2.0 host controller
- Supports HS (480Mbits/sec) and FS (12Mbits/sec) and LS (1.5Mbits/sec) Serial Transfer
- Supports Legacy Keyboard and Mouse Software with USB-based Keyboard and Mouse
- Support USB Wakeup from S1-S5 State

Key Feature of Legacy/LPC Controller

- Low Pin Count interface Spec.1.0 compliant
- Integrated System Peripherals(ISP).
  - 2 x 8237A ; 2 x 8259A ; 1 x 8254
- Support Common Architecture
  - Serialized IRQ ; Distribute DMA
- SMBus Host Controller
  - System Management Bus Interface Spec. 2.0 Compliant
  - Supports SMBALERT# Signal for Slave Device
- IO APIC (Advanced Programmable Interrupt Controller)
  - Expand the number of interrupts to 24
- Support 3 multi-media Timers

I/O Trends

- Chipset Southbridge define I/O of the system
  - Which I/O functions integrate depends on market demand
- I/O moves from Parallel to high speed Serial to save pins, cost and user friendly
  - PCI -> Hyper Transport, 3GIO
  - SIO -> USB, 1394
  - ATA -> Serial ATA
- High-speed Wireless Interface Technology
  - 802.11, Bluetooth™ just another form of I/O

Conclusion

- ALi will provide HyperTransport™ Technology South Bridge for PC, Work Station, Consumer application integrated with I/O of today and high speed serial I/O of the future